CERTIFICATION OF TRANSLATION

I, ***Donggy Sohn***, an employee of Y.P. LEE, MOCK & PARTNERS of The Cheonghwa Bldg., 1571-18 Seocho-dong, Seocho-gu, Seoul, Republic of Korea, hereby declare under penalty of perjury that I understand the Korean language and the English language; that I am fully capable of translating from Korean to English and vice versa; and that, to the best of my knowledge and belief, the statement in the English language in the attached translation of ***Korean Patent Application No. 10-2003-0006364*** consisting of 27 pages, have the same meanings as the statements in the Korean language in the original document, a copy of which I have examined.

Signed this 14th day of January 2006

ABSTRACT

[Abstract of the Disclosure]

Provided are a voltage controlled oscillator having a constant gain at a wide frequency band, and a method of operating the same. The voltage controlled oscillator is an inductor-capacitor (LC) voltage controlled oscillator that simultaneously uses switched capacitors and varactors. The oscillator generates an amplified oscillation signal having an oscillation frequency, which change in response to changes in input whole inductance and capacitance, and outputs the signal to an oscillation signal output terminal. The capacitances of the varactors change the moment the capacitances of the switched capacitors change. Accordingly, the oscillator has low-noise characteristics and the frequency bandwidth and gain of the oscillator are maintained regardless of the number of the switched capacitors or an increase in their capacitances. Therefore, when the oscillator is included into a PLL, the oscillator can stably operate.

[Representative Drawing]

FIG. 2

SPECIFICATION

[Title of the Invention]

WIDE-BAND VOLTAGE CONTROLLED OSCILLATOR WITH CONSTANT GAIN AND METHOD THEREOF

[Brief Description of the Drawings]

The present invention will become more apparent by describing in detail preferred embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a schematic circuit diagram of a conventional inductor-capacitor (LC) voltage controlled oscillator;

FIG. 2 is a circuit diagram of a voltage controlled oscillator according to a preferred embodiment of the present invention;

FIG. 3 is a graph illustrating a variation in the frequency of the voltage controlled oscillator of FIG. 2 versus a change in control voltage V_{cnt};

FIG. 4 is a graph illustrating a variation in a gain of the voltage controlled oscillator of FIG. 2 versus a change in the control voltage V_{cnt};

FIG. 5 is a graph illustrating a variation in a gain of the voltage controlled oscillator of FIG. 2 versus a change in a digital control signal and a fixed control voltage V_{cnt};

FIG. 6 is a graph illustrating a variation in a gain of the voltage controlled oscillator of FIG. 2 versus a change in a unit area of a switched varactor unit and a change in the digital control signal;

FIG. 7 is a circuit diagram of the voltage controlled oscillator of FIG 2 that is a complementary metal oxide semiconductor (CMOS), according to another embodiment of the present invention; and

FIG. 8 is a detailed circuit diagram of a capacitor bank unit of FIG. 7.

[Detailed Description of the Invention]

[Object of the Invention]

[Technical Field of the Invention and Related Art prior to the Invention]

The present invention relates to a voltage controlled oscillator, and more particularly, to an inductor-capacitor (LC) voltage controlled oscillator and a method using the same.

In general, mobile communication systems use an inductor-capacitor (LC) voltage controlled oscillator that includes an inductor and a varactor. In particular, the LC voltage controlled oscillator has frequency variable characteristics and low noise characteristics and thus is used as a local oscillator in mobile communication systems.

A demand for multi-band and multi-mode characteristics of an Integrated Circuit (IC) for communication led to a remarkable increase in the working frequency band of a voltage controlled oscillator. The voltage controlled oscillator is used as a local oscillator in a Phase-Locked Loop (PLL) of a communication system and also used in an offset PLL of a system transmission site such as a Global System for Mobile (GSM) communication. Therefore, the stability of the voltage controlled oscillator must be improved to stably operate the PLL. For an improvement in the stability of the PLL, a gain of the voltage controlled oscillator must be changed within a limited range at a wide working frequency band.

FIG. 1 is a schematic circuit diagram of a conventional LC voltage controlled oscillator.

Referring to FIG. 1, when application of a voltage to the conventional LC voltage controlled oscillator changes the capacitance *Cv* of a varactor, a whole capacitance of said oscillator changes but a whole inductance is fixed. In this case, a resonance frequency changes and leads to the LC voltage controlled oscillator to operate. In FIG. 1, *R* and C_{load} denote a parasitic resistance component and a capacitance component, which exist at a terminal of said oscillator that outputs an oscillation signal *Vo*.

In addition to the oscillator of FIG. 1, an LC voltage controlled oscillator that simultaneously uses a switched capacitor and a varactor can be used in mobile

communication systems. Such an oscillator is disclosed in US Patent No. 006,211,745 B1.

In the LC voltage controlled oscillator as shown in FIG. 1, the bandwidth of an oscillating frequency can be enlarged by increasing a range of the capacitance *Cv* of the varactor. However, a gain of said oscillator must be increased to widen the range of the capacitance Cv of a varactor. However, an excessive increase in the gain of said oscillator aggravates the noise characteristics of said oscillator. Further, as ICs have been developed to operate at a low voltage, there is a limit to increase the frequency bandwidth of an oscillator that uses a varactor.

Meanwhile, since a switched capacitor and a varactor are simultaneously used to enlarge the frequency bandwidth of a conventional LC voltage controlled oscillator, an increase in a total number of switched capacitors increases the bandwidth of a working frequency but causes fluctuation of a gain of the oscillator. Accordingly, the use of the oscillator in a PLL deteriorates the stability of the oscillator.

[Technical Goal of the Invention]

The present invention provides an improvement of an inductor-capacitor (LC) voltage controlled oscillator that uses a switched capacitor unit and a varactor unit simultaneously, the improvement enabling the capacitance of the varactor unit to change when the capacitance of the switched capacitor unit changes, thus maintaining a gain of the oscillator even at a wide frequency band.

The present invention also provides a method of maintaining a gain of an LC voltage controlled oscillator at a wide frequency band by changing the capacitance of a varactor unit when the capacitance of a switched capacitor unit changes.

[Structure and Operation of the Invention]

According to an aspect of the present invention, there is provided a voltage controlled oscillator comprising a trans-conductance amplifier that generates an amplified oscillation signal having oscillation frequency, which change in response to

changes in input whole inductance and capacitance, and outputs the signal to an oscillation signal output terminal; an inductor that supplies the whole inductance; a non-switched varactor whose capacitance changes in accordance with a change in a control voltage applied to a control voltage input terminal, the capacitance of the non-switched varactor resulting in a change in the whole capacitance; a switched capacitor unit that includes a plurality of digital switches controlled by a control circuit, and capacitors connected to the digital switches, respectively, the capacitances of the capacitors connected to the switched digital switches being adjusted to change the whole capacitance; and a switched varactor unit that includes a plurality of digital switches, and varactors that are connected to the digital switches, respectively, and whose capacitances change in accordance with a change in the control voltage, the capacitances of the varactors connected to the switched digital switches being adjusted to change the whole capacitance.

The trans-conductance amplifier may include a bipolar transistor or a field effect transistor.

The switched capacitor unit comprises the plurality of capacitors, the capacitances of which are assigned with binary weights to obtain capacitance values C_{SW}, 2^1C_{SW},..., and $2^{(n-1)}C_{SW}$, C_{SW} denoting the capacitance value of the lowest-rank capacitor.

The switched varactor unit comprises the plurality of varactors, the capacitances of which are assigned with binary weights to obtain capacitance values $C_{V,SW}$, $2^1C_{V,SW}$,..., and $2^{n-1}C_{V,SW}$, $C_{V,SW}$ denoting the capacitance value of the lowest-rank varactor.

The varactors included in the switched varactor unit are means that change in accordance with a change in the control voltage. In particular, the varactors included in the switched varactor unit have pn-unction diode structures such that their capacitances change in accordance with a change in the control voltage.

The control circuit generates a digital control signal for switching on/off the digital switches so as to appropriately set a capacitance area of the switched varactor, thereby minimizing a ratio of a gain variation of the oscillator to the total capacitance.

In particular, switching on or off of the digital switches is controlled such that the capacitances of the varactors of the switched varactor unit connected to switched digital switches satisfy the following equation:

$$C_{v,k} = (A_0 + k.A_{sw}).C_{jo}.(1 + V_{cnt}/\phi)^{-m}$$

wherein *k* denotes a decimal value of a binary digital control signal value, $C_{v,k}$ denotes a sum of the capacitances of the varactors connected to switched digital switches, A_o denotes a capacitance area of a non-switched varactor, A_{sw} denotes a unit capacitance area of a switched varactor, V_{cnt} denotes an input control voltage, C_{jo} denotes a capacitance value per a unit area of a varactor when an inverse bias voltage is 0, ϕ denotes a built-in potential, and *m* denotes a coefficient that represents varactor characteristics,

wherein the unit capacitance area of the switched varactor A_{sw} is computed to minimize the rate of variation in a gain of the oscillator using the following equations:

$$Q = -\frac{(1+\frac{C_d}{C_{v,k}})^2}{9}, \quad R = -\frac{27.(\frac{C_d + C_{sw}}{C_{v,k}}) + 2.(1+\frac{C_d}{C_{v,k}})^3}{54},$$

$$S = \sqrt[3]{R + \sqrt{Q^3 + R^2}}, \; T = \sqrt[3]{R - \sqrt{Q^3 + R^2}}, \; where \; S.T = -Q,$$

$$a = (S + T + (\frac{1}{3}).(1+\frac{C_d}{C_{v,k}}))^3 = \frac{A_0 + (k+1).A_{sw}}{A_0 + k.A_{sw}},$$

$$A_{sw} = \frac{A_0.(a-1)}{k.(1-a)+1}$$

where *Cd* denotes a load capacitance value that is parasitic on an oscillation signal output terminal, *k* denotes a decimal value of a binary digital control signal value, $C_{v,k}$ denotes a sum of the capacitances of varactors connected to switched digital switches, C_{sw} denotes a capacitance value of switched capacitors, A_o denotes a capacitance area

of a non-switched varactor, and A_{sw} denotes a unit capacitance area of a switched varactor.

According to another aspect of the present invention, there is provided a method of operating a voltage controlled oscillator, the method comprising supplying a whole inductance using an inductor included in the oscillator; changing the whole capacitance of the oscillator by controlling the capacitance of a varactor unit included in the oscillator in accordance with a change in a control voltage input to a control voltage input terminal; changing the whole capacitance of the oscillator by controlling a sum of the capacitances of a plurality of capacitors of a switched capacitor unit connected to a plurality of switched digital switches, the plurality of digital switches being controlled by a control circuit; changing the whole capacitance of the oscillator by controlling a sum of the capacitances of a plurality of varactors of a switched varactor unit connected to the switched digital switches, the capacitances of the varactors changing in accordance with a change in the control voltage; and generating an amplified oscillation signal having oscillation frequency, which change in response to changes in the input whole inductance and capacitance, using a trans-conductance amplifier included in the oscillator, and outputting the signal to an oscillation signal output terminal.

In a voltage controlled oscillator according to the present invention, a trans-conductance (Gm) amplifier generates an amplified oscillation signal V_o having oscillation frequency, which changes in response to changes in a whole inductance and a whole capacitance, and outputs the signal V_0 to an oscillation signal output terminal, i.e., a V_o node.

Hereinafter, preferred embodiments of the present invention will be described in detail with reference to the accompanying drawings. The same reference numerals represent the same elements throughout the drawings.

FIG. 2 is a circuit diagram of a voltage controlled oscillator according to a preferred embodiment of the present invention. Referring to FIG. 2, the voltage controlled oscillator includes a trans-conductance (Gm) amplifier 100, an inductor 110, a non-switched varactor unit 120, a switched capacitor unit 130, and a switched varactor

unit 140. In FIG. 2, C_d denotes a different capacitance component that is parasitic on an oscillation signal output terminal, and R denotes a different resistance component that is also parasitic on the oscillation signal output terminal.

The trans-conductance (Gm) amplifier 100 generates an amplified oscillation signal V_o having oscillation frequency that changes in accordance with in an input whole inductance and capacitance, and outputs the oscillation signal V_o to the oscillation signal output terminal. In this embodiment, the trans-conductance (Gm) amplifier 100 includes a bipolar transistor but may include a field effect transistor (FET) instead of the bipolar transistor.

The inductor 110 supplies the whole inductance.

The capacitance of the non-switched varactor unit 120 changes when a control voltage V_{cnt} applied to a control voltage input terminal changes, thus resulting in a change in the whole capacitance.

The switched capacitor unit 130 includes a plurality of digital switches SW_0 through SW_{n-1} that are controlled by a control circuit (not shown), and a plurality of capacitors connected to the switches SW_0 through SW_{n-1}, respectively. Also, the capacitance of the switched capacitor unit 130 is determined by a sum of the capacitances of the capacitors connected to the switched digital switches SW_0 through SW_{n-1} and the whole capacitance depends on the capacitance of the switched capacitor unit 130. As shown in FIG. 2, binary weights are applied to capacitance values of the capacitors of the switched capacitor unit 130, and thus, their capacitance values are C_{SW}, 2^1C_{SW}, ..., and $2^{n-1}C_{SW}$. Here, C_{SW} denotes the capacitance value of the lowest-rank capacitor.

The switched varactor unit 140 includes a plurality of digital switches SW_0 through SW_{n-1} and a plurality of varactors connected to the digital switches SW_0 through SW_{n-1}, respectively. A change in the control voltage V_{cnt} results in a change in the capacitances of the varactors. The capacitance of the switched varactor unit 140 is determined by a sum of the capacitances of the varactors connected to the switched digital switches SW_0 through SW_{n-1}, and the whole capacitance also depends on the

capacitance of the switched varactor unit 140. As shown in FIG. 2, binary weights are applied to capacitance values of the varactors of the switched varactor unit 140, and thus, their capacitance values are $C_{V,SW}$, $2^1C_{V,SW}$,..., and $2^{n-1}C_{V,SW}$. $C_{V,SW}$ denotes the capacitance value of the lowest-rank varactor. The varactors of the switched varactor unit 140 are means that change depending on a change in the control voltage V_{cnt}. In particular, the varactors have pn-junction diode structures and their capacitances change in accordance with a change in the control voltage V_{cnt}.

The control circuit generates a digital control signal for switching on or off the digital switches SW_0 through SW_{n-1} included in the switched capacitor unit 130 and the switched varactor unit 140 so as to adjust the capacitance area of the switched varactor unit 140, thereby controlling the whole capacitance of the oscillator and minimizing a variation in a gain of the oscillator. More specifically, switching on or off of digital switches SW_0 through SW_{n-1} is controlled such that a sum of the capacitances of the capacitors connected to switched digital switches satisfies Equation (4). A gain of the oscillator is computed using Equations (1) and (2) and the unit capacitance area of a switched varactor is computed using Equation (3).

$$
\begin{aligned}
&F = \frac{1}{2\pi\sqrt{LC}}\,,\\
&C = Cv + k \times Csw + Cd\,,\\
&Cv = A.C_{jo}.(1+V_{cnt}/\phi)^{-m}\,,\\
&K_{vco} = \frac{\partial F}{\partial V_{cnt}}\\
&\quad = \frac{\partial F}{\partial C_v}.\frac{\partial C_v}{\partial V_{cnt}}\\
&\quad = \frac{1}{4\pi.\sqrt{L}}(C_d + k.C_{sw} + C_v)^{-3/2}.(-m).A.C_{jo}.(1+V_{cnt}/\phi)^{-<m+1)}\\
&\quad = \frac{A.C_{jo}.m}{4\pi.\sqrt{L}}(C_d + k.C_{sw} + C_v)^{-3/2}.(1+V_{cnt}/\phi)^{-(m+1)}.(1/\phi)
\end{aligned}
\qquad \ldots (1),
$$

wherein F denotes oscillation frequency; L denotes an inductance value of an inductor; C denotes a whole conductance value; C_d denotes a load capacitance value

that is parasitic on an oscillation signal output terminal; k denotes a decimal value of a binary digital control signal value, ranging from 0 to 2^{n-1}; C_v denotes a sum of the capacitance values of the varactors connected to switched digital switches SW_0 through SW_{n-1}; C_{sw} denotes a capacitance value of a switched capacitor; K_{vco} denotes a gain of the oscillator; A denotes a capacitance area of a varactor; V_{cnt} denotes an input control voltage; C_{jo} denotes a capacitance value per a unit area of a varactor when an inverse bias voltage is 0; ϕ denotes a built-in potential; and m denotes a coefficient that represents varactor characteristics.

$$K_{vco,k} = \frac{(A_0 + k.A_{sw}).C_{jo}.m}{\phi.4\pi.\sqrt{L}}(C_d + k.C_{sw} + C_{vk})^{-3/2}.(1+V_{cnt}/\phi)^{-(M+1)}.(1/\phi) \quad \ldots (2),$$

wherein A_0 denotes a capacitance area of a non-switched varactor and A_{sw} denotes a unit capacitance area of a switched varactor.

$$Q = -\frac{(1+\frac{C_d}{C_{v,k}})^2}{9}, \quad R = -\frac{27.(\frac{C_d + C_{sw}}{C_{v,k}}) + 2.(1+\frac{C_d}{C_{v,k}})^3}{54},$$

$$S = \sqrt[3]{R + \sqrt{Q^3 + R^2}}, \quad T = \sqrt[3]{R - \sqrt{Q^3 + R^2}}, \quad where\ S.T = -Q,$$

$$a = (S + T + (\frac{1}{3}).(1+\frac{C_d}{C_{v,k}}))^3 = \frac{A_0 + (k+1).A_{sw}}{A_0 + k.A_{sw}},$$

$$A_{sw} = \frac{A_0.(a-1)}{k.(1-a)+1}$$

... (3),

where C_d denotes a load capacitance value that is parasitic on an oscillation signal output terminal; k denotes a decimal value of a binary digital control signal value; $C_{v,k}$ denotes a sum of the capacitance values of varactors connected to switched digital switches SW_0 through SW_{n-1}; C_{sw} denotes a capacitance value of switched capacitors; A_o denotes a capacitance area of a non-switched varactor; and A_{sw} denotes a unit capacitance area of a switched varactor.

Equation (3) is based on $K_{vco,k} = K_{vco,k+1}$, that is, the gain $K_{vco,k}$ of the oscillator enclosed in Equation (2) has a constant value regardless of the decimal value k.

The sum $C_{v,k}$ enclosed in Equation (3) must satisfy Equation (4):

$$C_{v,k} = (A_0 + k.A_{sw}).C_{jo}.(1 + V_{cnt}/\phi)^{-m} \quad \ldots (4),$$

wherein k denotes a decimal value of a binary digital control signal value; $C_{v,k}$ denotes a sum of the capacitance values of varactors connected to switched digital switches SW_0 through SW_{n-1}; A_o denotes a capacitance area of a non-switched varactor; A_{sw} denotes a unit capacitance area of a switched varactor; V_{cnt} denotes an input control voltage; C_{jo} denotes a capacitance value per a unit area of a varactor when an inverse bias voltage is 0; ϕ denotes a built-in potential; and m denotes a coefficient that represents varactor characteristics.

As mentioned above, the control circuit determines the unit capacitance area A_{sw} of a switched varactor using Equation (3) so as to minimize a variation in a gain of the oscillator versus a change in the decimal value k. Even if a gain of the oscillator decreases due to the capacitance of the switched capacitor unit 130, it is possible to compensate for the gain by adjusting the capacitances of the varactors of the switched varactor unit 140. Accordingly, the gain of the oscillator can be maintained even at a wide working frequency band.

For this reason, the frequency bandwidth and gain of the oscillator according to the present invention can be maintained even at a wide frequency band regardless of the number of capacitors of the switched capacitor unit and an increase in their capacitances. Therefore, the oscillator according to the present invention can operate stably in phase-locked loop (PLL).

FIG. 3 is a graph illustrating a variation in the frequency characteristics of the voltage controlled oscillator of FIG. 2 versus a change in a control voltage V_{cnt}.

In detail, the graph of FIG. 3 shows the result of a simulation where a variation in the frequency characteristics of the voltage controlled oscillator of FIG. 2 was measured with three digital switches, three capacitors, and three varactors. Here, *Freq0* through *Freq7* indicate frequency characteristics, respectively, when a decimal value k of a binary digital control signal value ranges from 0 to 7. Referring to FIG. 3, the working frequency of a voltage controlled oscillator according to the present invention increases to a small extent as a control voltage V_{cnt} increases.

FIG. 4 is a graph illustrating a variation in a gain of the voltage controlled oscillator of FIG. 2 versus a change in a control voltage V_{cnt}.

The graph of FIG. 4 shows the result of a simulation where a variation in the frequency characteristics of the voltage controlled oscillator of FIG. 2 was measured with three digital switches, three capacitors, and three varactors. Here, $K_{vco}0$ through $K_{vco}7$ indicate the gain of the oscillator, respectively, when a decimal value k of a binary digital control signal value ranges from 0 to 7. Referring to FIG. 4, a gain of a voltage controlled oscillator according to the present invention is almost uniformly maintained regardless of working frequency in a control voltage V_{cnt}.

FIG. 5 is a graph illustrating a variation in a gain of the voltage controlled oscillator of FIG. 2 with respect to a change in a digital control signal value when control voltage V_{cnt} is fixed.

The graph of FIG. 5 shows the result of a simulation where a variation in a gain of the voltage controlled oscillator of FIG. 2 was measured with three digital switches, three capacitors, and three varactors when a decimal value k of a binary digital control signal value ranges from 0 to 7. Referring to FIG. 5, the rate of variation in a gain of a voltage controlled oscillator according to the present invention is very small when the decimal value k is small but becomes slightly increases as the decimal value k becomes larger. In conclusion, when decimal value k changes ranging from 0 to 7, the rate of variation in a gain of the oscillator according to the present invention is 8%, that is, it is very minimal.

FIG. 6 is a graph illustrating a variation in a gain of the voltage controlled oscillator of FIG. 2 when a unit area A_{sw} of a switched varactor and a digital control signal value change.

The graph of FIG. 6 shows the result of a simulation where a variation in a gain of the voltage controlled oscillator of FIG. 2 was measured with three digital switches, three capacitors, and three varactors when a decimal value k of a binary digital control signal value changes ranging from 0 to 7. As previously mentioned, A_{sw} denotes a unit capacitance area of a switched varactor. FIG. 6 shows the gains $K_{vco,k}$ of the oscillator

when the capacitance areas A_{sw} are 3.5, 4, 4.5, and 5. It is preferable that the capacitance area A_{sw} is 4.5 where the rate of variation in a gain of the oscillator is very small, i.e., 4%.

FIG. 7 is a circuit diagram of the voltage controlled oscillator of FIG 2 that is a complementary metal oxide semiconductor (CMOS), according to another embodiment of the present invention. FIG. 8 is a detailed circuit diagram of a capacitor bank 730 of FIG. 7.

Referring to FIG. 7, the oscillator according to another embodiment of the present invention includes a trans-conductance (Gm) amplifier 700, an inductor 710, a non-switched varactor unit 720, and the capacitor bank 730. Referring to FIG. 8, the capacitor bank 730 includes a switched capacitor unit 731 and a switched varactor unit 733. The operations of these elements are the same as those of the elements of FIG. 2, and thus, their descriptions will be omitted here.

The operation and structure of the voltage controlled oscillator shown in FIGS. 7 and 8 are equivalent to those of the voltage controlled oscillator of FIG. 2, except that the capacitor bank 730 is further included and the switched capacitor unit 731 and the switched varactors 733 are installed in the capacitor bank 730.

Here, D_0 through D_{n-1} denote signals for switching on or off a plurality of digital switches (not shown), shown in FIG. 8, which are installed in the switched varactor unit 733. The signals D_0 through D_{n-1} are generated by a control circuit described with reference to FIG. 2. In the voltage controlled oscillator of FIGs. 7 and 8, the trans-conductance (Gm) amplifier 700 generates an amplified oscillation signals V_0^+ and V_0^- whose oscillation frequencies change in response to input whole inductances *L1* and *L2* and a whole capacitance, i.e., a sum of the capacitance C_v of the non-switched varactor unit 720 and the capacitance of the capacitor bank 730. The oscillation signals V_0^+ and V_0^- are output to oscillation signal output terminals, i.e., nodes V_0^+ and V_0^-.

Like in FIG. 2, the control circuit generates the signals D_0 through D_{n-1} for controlling switching on or off of the digital switches so as to adjust the capacitance area of the switched varactor unit 733, thereby controlling the whole capacitance and minimizing the rate of variation in a gain of the oscillator.

As described with respect to FIG. 2, switching on or off of digital switches is controlled such that the capacitance area of the switched varactor unit is adjusted to minimize the rate of variation in the gain of the oscillator. A gain of the oscillator is computed using Equations (1) and (2) and the unit capacitance area of a switched varactor is computed using Equation (3). The sum $C_{v,k}$ enclosed in Equation (3) must satisfy Equation (4). Equation (3) is based on $K_{vco,k} = K_{vco,k+1}$, that is, the gain $K_{vco,k}$ of the oscillator enclosed in Equation (2) has a fixed value regardless of the decimal value k. However, unlike in the oscillator of FIG. 2, the switched capacitor unit 731 and the switched varactor unit 733 have symmetrical structures, and therefore, the capacitance of each of them in Equations (1) through (4) corresponds to the one-side total capacitance of respective switched capacitors and varactors.

In conclusion, in a voltage controlled oscillator according to the present invention, a trans-conductance (Gm) amplifier generates an amplified oscillation signal V_o having oscillation frequency, which changes in response to changes in a whole inductance and a whole capacitance, and outputs the signal V_0 to an oscillation signal output terminal, i.e., a V_o node. Next, an inductor supplies the whole inductance. The capacitance of a non-switched varactor unit changes according to a change in a control voltage V_{cnt} applied to an oscillation signal input terminal, resulting in a change in the whole capacitance. A switched capacitor unit includes a plurality of digital switches controlled by a control circuit and includes a plurality of capacitors connected to the digital switches, respectively. The capacitance of the switched capacitor unit is adjusted by a sum of the capacitances of the capacitors connected to the switched digital switches, resulting in a change of the whole capacitance. The switched varactor unit includes a plurality of digital switches and a plurality of varactors connected to the digital switches, the capacitances of the varactors changing according to a change in the control voltage

V_{cnt}. The capacitance of the switched varactor unit 140 is also adjusted by a sum of the capacitances of the varactors connected to the switched digital switches, resulting in a change in the whole capacitance.

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

[Effect of the Invention]

As describe above, a voltage controlled oscillator according to the present invention is an inductor-capacitor (LC) voltage controlled oscillator that simultaneously uses switched capacitors and varactors, the oscillator being designed such that the capacitances of the varactors change the moment the capacitances of the switched capacitors change. Accordingly, the oscillator has low-noise characteristics and operates at a wide frequency band even if a low-level supply voltage is applied to an integrated circuit (IC). Further, the frequency bandwidth and gain of the oscillator are maintained regardless of the number of the switched capacitors or an increase in their capacitances. Therefore, when the oscillator is included into a PLL, the oscillator can stably operate.

What is claimed is:

1. A voltage controlled oscillator comprising:

a trans-conductance amplifier that generates an amplified oscillation signal having oscillation frequency, which change in response to changes in input whole inductance and capacitance, and outputs the signal to an oscillation signal output terminal;

an inductor that supplies the whole inductance;

a non-switched varactor whose capacitance changes in accordance with a change in a control voltage applied to a control voltage input terminal, the capacitance of the non-switched varactor resulting in a change in the whole capacitance;

a switched capacitor unit that includes a plurality of digital switches controlled by a control circuit, and capacitors connected to the digital switches, respectively, the capacitances of the capacitors connected to the switched digital switches being adjusted to change the whole capacitance; and

a switched varactor unit that includes a plurality of digital switches, and varactors that are connected to the digital switches, respectively, and whose capacitances change in accordance with a change in the control voltage, the capacitances of the varactors connected to the switched digital switches being adjusted to change the whole capacitance.

2. The oscillator of claim 1, wherein the trans-conductance amplifier comprises a bipolar transistor.

3. The oscillator of claim 1, wherein the trans-conductance amplifier comprises a field effect transistor.

4. The oscillator of claim 1, wherein the switched capacitor unit comprises the plurality of capacitors, the capacitances of which are assigned with binary weights to obtain capacitance values C_{SW}, 2^1C_{SW},..., and $2^{(n-1)}C_{SW}$, C_{SW} denoting the capacitance

value of the lowest-rank capacitor.

5. The oscillator of claim 1, wherein the switched varactor unit comprises the plurality of varactors, the capacitances of which are assigned with binary weights to obtain capacitance values $C_{V,SW}$, $2^1C_{V,SW}$,..., and $2^{n-1}C_{V,SW}$, $C_{V,SW}$ denoting the capacitance value of the lowest-rank varactor.

6. The oscillator of any one of claims 1 and 5, wherein the varactors included in the switched varactor unit are means that change in accordance with a change in the control voltage.

7. The oscillator of any one of claims 1 and 5, wherein the varactors included in the switched varactor unit have pn-unction diode structures such that their capacitances change in accordance with a change in the control voltage.

8. The oscillator of claim 1, wherein the control circuit switches on or off the digital switches such that the whole capacitance is adjusted to minimize the rate of variation in a gain of the oscillator.

9. The oscillator of any one of claims 1 and 8, wherein switching on or off of the digital switches is controlled such that the capacitances of the varactors of the switched varactor unit connected to switched digital switches satisfy the following equation:

$$C_{v,k} = (A_0 + k.A_{sw}).C_{jo}.(1 + V_{cnt}/\phi)^{-m}$$

wherein k denotes a decimal value of a binary digital control signal value, $C_{v,k}$ denotes a sum of the capacitances of the varactors connected to switched digital switches, A_o denotes a capacitance area of a non-switched varactor, A_{sw} denotes a unit capacitance area of a switched varactor, V_{cnt} denotes an input control voltage, C_{jo} denotes a capacitance value per a unit area of a varactor when an inverse bias voltage

is 0, ϕ denotes a built-in potential, and m denotes a coefficient that represents varactor characteristics,

wherein the unit capacitance area of the switched varactor A_{sw} is computed to minimize the rate of variation in a gain of the oscillator using the following equations:

$$Q = -\frac{(1+\frac{C_d}{C_{v,k}})^2}{9}, \quad R = -\frac{27.(\frac{C_d + C_{sw}}{C_{v,k}}) + 2.(1+\frac{C_d}{C_{v,k}})^3}{54},$$

$$S = \sqrt[3]{R + \sqrt{Q^3 + R^2}}, \; T = \sqrt[3]{R - \sqrt{Q^3 + R^2}}, \; where \; S.T = -Q,$$

$$a = (S + T + (\frac{1}{3}).(1+\frac{C_d}{C_{v,k}}))^3 = \frac{A_0 + (k+1).A_{sw}}{A_0 + k.\,A_{sw}},$$

$$A_{sw} = \frac{A_0.(a-1)}{k.(1-a)+1}$$

where *Cd* denotes a load capacitance value that is parasitic on an oscillation signal output terminal, *k* denotes a decimal value of a binary digital control signal value, $C_{v,k}$ denotes a sum of the capacitances of varactors connected to switched digital switches, C_{sw} denotes a capacitance value of switched capacitors, A_o denotes a capacitance area of a non-switched varactor, and A_{sw} denotes a unit capacitance area of a switched varactor.

10. A method of operating a voltage controlled oscillator, comprising:

supplying a whole inductance using an inductor included in the oscillator;

changing the whole capacitance of the oscillator by controlling the capacitance of a varactor unit included in the oscillator in accordance with a change in a control voltage input to a control voltage input terminal;

changing the whole capacitance of the oscillator by controlling a sum of the capacitances of a plurality of capacitors of a switched capacitor unit connected to a plurality of switched digital switches, the plurality of digital switches being controlled by a control circuit;

changing the whole capacitance of the oscillator by controlling a sum of the capacitances of a plurality of varactors of a switched varactor unit connected to the

switched digital switches, the capacitances of the varactors changing in accordance with a change in the control voltage; and

generating an amplified oscillation signal having oscillation frequency, which change in response to changes in the input whole inductance and capacitance, using a trans-conductance amplifier included in the oscillator, and outputting the signal to an oscillation signal output terminal.

11. The method of claim 10, wherein the trans-conductance amplifier comprises a bipolar transistor.

12. The method of claim 10, wherein the trans-conductance amplifier comprises a field effect transistor.

13. The method of claim 10, wherein the switched capacitor unit comprises the plurality of capacitors, the capacitances of which are assigned with binary weights to obtain capacitance values C_{SW}, 2^1C_{SW},..., and $2^{(n-1)}C_{SW}$, C_{SW} denoting the capacitance value of the lowest-rank capacitor.

14. The method of claim 10, wherein the switched varactor unit comprises the plurality of varactors, the capacitances of which are assigned with binary weights to obtain capacitance values $C_{V,SW}$, $2^1C_{V,SW}$,..., and $2^{(n-1)}C_{V,SW}$, $C_{V,SW}$ denoting the capacitance value of the lowest-rank varactor.

15. The method of any one of claims 10 and 14, wherein the varactors included in the switched varactor unit are means that change in accordance with a change in the control voltage.

16. The method of any one of claims 10 and 14, wherein the varactors included in switched varactor unit have pn-junction diode structures such that their

capacitances change in accordance with a change in the control voltage.

17. The method of claim 10, wherein the control circuit switches on or off the digital switches such that the whole capacitance is controlled to minimize the rate of variation in a gain of the oscillator.

18. The method of any one of claims 10 and 17, wherein switching on or off of the digital switches is controlled such that the capacitances of the varactors of the switched varactor unit connected to switched digital switches satisfy the following equation:

$$C_{v,k} = (A_0 + k.A_{sw}).C_{jo}.(1+V_{cnt}/\phi)^{-m}$$

wherein *k* denotes a decimal value of a binary digital control signal value, $C_{v,k}$ denotes a sum of the capacitances of the varactors connected to switched digital switches, A_o denotes a capacitance area of a non-switched varactor, A_{sw} denotes a unit capacitance area of a switched varactor, V_{cnt} denotes an input control voltage, C_{jo} denotes a capacitance value per a unit area of a varactor when an inverse bias voltage is 0, ϕ denotes a built-in potential, and *m* denotes a coefficient that represents varactor characteristics,

wherein the unit capacitance area of the switched varactor A_{sw} is computed to minimize the rate of variation in a gain of the oscillator using the following equations:

$$Q = -\frac{(1+\frac{C_d}{C_{v,k}})^2}{9}, \quad R = -\frac{27.(\frac{C_d+C_{sw}}{C_{v,k}}) + 2.(1+\frac{C_d}{C_{v,k}})^3}{54},$$

$$S = \sqrt[3]{R+\sqrt{Q^3+R^2}}, \; T = \sqrt[3]{R-\sqrt{Q^3+R^2}}, \; where \; S.T = -Q,$$

$$a = (S+T+(\frac{1}{3}).(1+\frac{C_d}{C_{v,k}}))^3 = \frac{A_0+(k+1).A_{sw}}{A_0+k.A_{sw}},$$

$$A_{sw} = \frac{A_0.(a-1)}{k.(1-a)+1}$$

where *Cd* denotes a load capacitance value that is parasitic on an oscillation signal

output terminal, k denotes a decimal value of a binary digital control signal value, $C_{v,k}$ denotes a sum of the capacitances of varactors connected to switched digital switches, C_{sw} denotes a capacitance value of switched capacitors, A_o denotes a capacitance area of a non-switched varactor, and A_{sw} denotes a unit capacitance area of a switched varactor.